SECTION 2 - Computer Controls

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COMPUTER CONTROLS

On the processor console is a set of data switches through which an operator can supply words and addresses to the program. This is :-

The Control Panel

The Manual Control Unit consists of a panel which is situated in the chassis. It provides all necessary manual control over the computer.

The panel includes the following set of control elements as indicated in Fig. 2:1 on the next page :-

1	Power On/Off pushbutton
1	Key Operated Security Lock
7	Power-Pack Indicators
27	Indicator Lamps
17	Data Switches
14	Control Switches

A functional description of each of these follows :-

The Power On/Off button should be pushed in to switch on the CPU - it will then lock in position and light up. To switch off, the button should be pushed once again.

The security lock is a two-position, Key operated locking switch which can disable all switches on the Panel except the 17 Data Switches, which can then only be accessed from program by the Register Instruction 'Enter Switch Register into Accumulator A or B'. This lock eliminates any accidental manual input to the system.

In the Normal position the Key is ejected and, when switched on, the Program will start from address 000002 (which is set on PC and MA) with Interrupt Off.

When in 'Manual' Mode, all Control Switches on the Panel are enabled. To change to Manual operation the Key should be inserted and turned towards 'Manual', leaving it in this position. The program will not then start automatically, although the PC and MA will be set to address 000002 when first switched on.

CONTROL PANEL

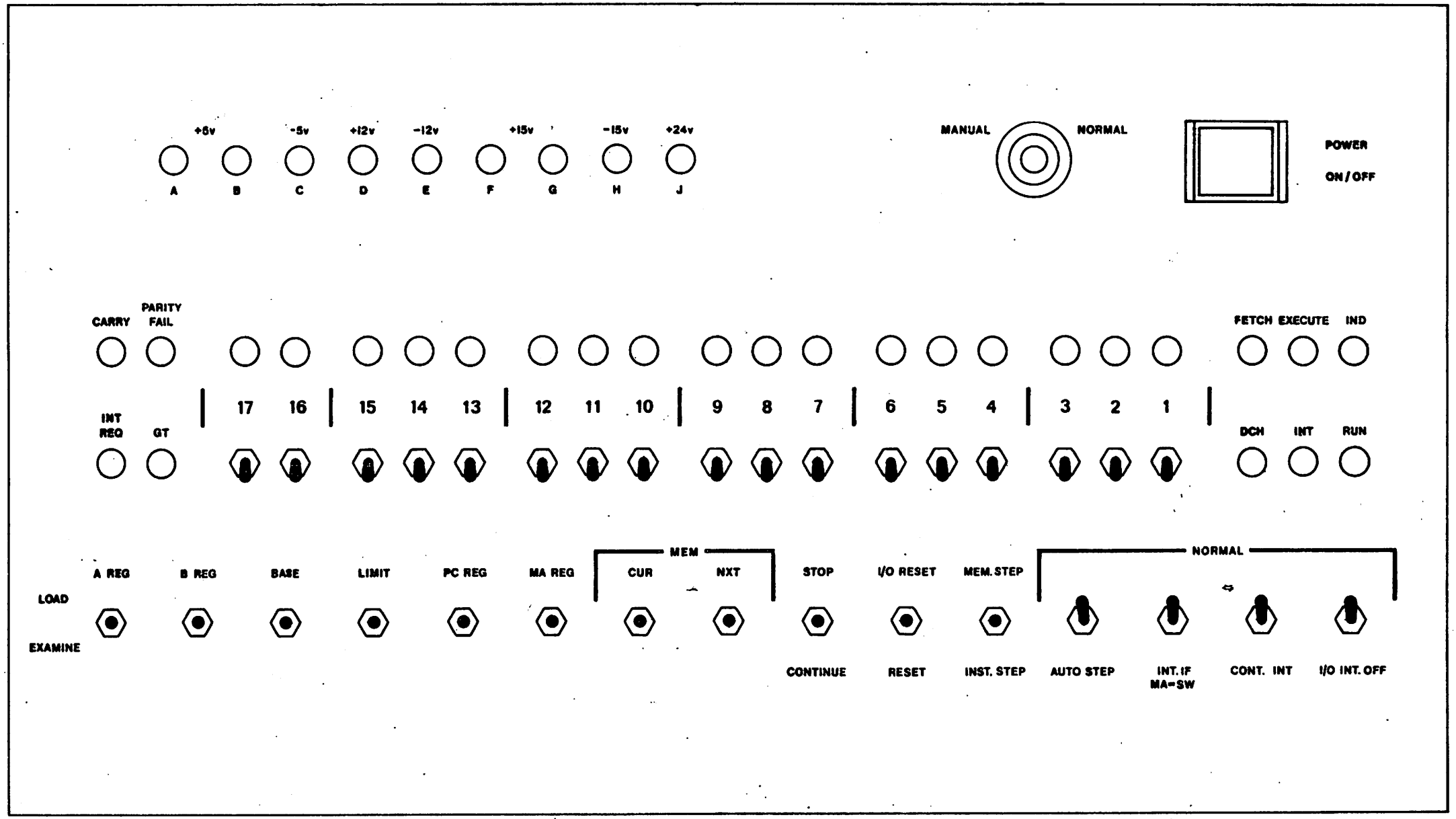

Fig.2.1

The 9 blue lights on the top left-hand side are power supply indicators.

The 6 lights on the right-hand side, below the Power On/Off button, display control conditions. A few of these indicators display useful information while the processor is running, but most change too frequently, and are therefore described in terms of the information they display when the processor has stopped.

The top 3 lights, Fetch, Execute and Indirect, also the DCH light in the bottom row, are phase indicators in that they specify the phase (the type of cycle) the processor will enter if operations are continued.

Fetch indicates that the next machine cycle will be used to 'Fetch' an instruction from memory.

Execute indicates that the next processor cycle will be used to reference memory for an operand in a move data or modify memory instruction.

Indirect indicates that the next processor cycle will be used to Fetch an address word in an indirectly addressed memory reference instruction.

DCH indicates that the next processor cycle will be used by data channel for direct access to memory by an in/out device.

Interrupt indicates that an Interrupt is being taken.

Run indicates that the processor is in normal operation with one instruction following another. This light goes off when 'Stop' is pressed, when a 'Halt' instruction is executed, or when an abnormal change occurs in the internal power supplies.

There are twenty-one (21) other indicator lights, nineteen of them being in a row above the Data switches. The red light on the extreme left-hand side is equivalent to the Carry flag. The red light next to it, when on, indicates a parity error has occurred in the memory system, the parity bit being used by the system for internal checking purposes.

The other 17 lights in this row are 'bit indicator' lights numbered 17 to 1 from left to right, forming a register with Bit 17 being the most significant and Bit 1 the least significant. This register can represent and display the contents of any hardware register or core location.

Below the bit indicator lights is a set of Data switches used for direct communication with the central processor. This is a set of 17 toggle switches used to specify binary numbers, which are then either loaded into the appropriate registers when other switches on the console are operated or loaded into an accumulator at Program command (ESWRA or ESWRB). The 17 positions represent a 17-bit binary word. When a switch is up it represents a binary '1' and is considered set; conversely, when a switch is down it represents a binary '0' and is considered reset.

Note :- The bit indicator lights do not change or light up as the Data switches are operated.

On the left of the Data switches two more indicator lights are situated. The one on the extreme left, when on, indicates that an Interrupt has been requested. The other indicator light is equivalent to the Greater Than flag.

The data switches may be used in conjunction with any of the 8 bottom row switches on the left hand side. These are operating or control switches and are interlocked so that if they are operated by mistake while the security lock is in the Normal position, they will have no adverse effect on the running program. Each of the operating switch levers is actually a three positional spring-loaded switch with a common off position in the centre. Lifting a switch lever up loads the contents of the data switches into the specified register. Pressing a switch down displays the contents in the bit indicator lights, thus enabling the user either to examine what has just been loaded or to examine the contents of the specified register.

e.g. Starting at the left-hand side:-

1) With switch labelled 'A.Reg', the operator can load and/or examine the contents of the A Register.

2) With switch labelled 'B.Reg', the operator can load and/or examine the contents of the B Register.

3) With switch labelled 'Base', the operator can load and/or examine the contents of the Base Register.

4) With switch labelled 'Limit', the operator can load and/or examine the contents of the Limit register.

5) With switch labelled 'P.C.Reg', the operator can load and/or examine the contents of the Program Counter, which represents the address of the next instruction to be fetched out of memory.

6) With switch labelled 'M.A.Reg', the operator can load and/or examine the Memory Address, which represents the address of the memory word being examined or loaded.

7) With switch labelled 'CUR', having previously loaded the Memory Address with the required address, the operator may now load the Memory Buffer and core with the contents of the data switches and/or examine the contents of the current location.

8) With switch labelled 'NXT' having once loaded the "Current" address with data from the switches, the operator may continue loading the next consecutive word by resetting the Data switches to the required pattern and pressing the 'NXT' switch up. This operation may be repeated as many times as necessary, because each Load operation of the 'NXT' switch increments the MA by 1.

Each of the next three switch levers is also a three positional spring-loaded switch with a common off position in the centre. Lifting the lever up initiates the condition printed above it. Pressing it down initiates the condition printed below :-

STOP When the switch is pressed up, the STOP switch halts program execution at the end of the instruction in progress, when the run light will go off.

CONTINUE When the switch is depressed, the run indicator light will be turned on, and the processor will begin normal operation, executing the instruction at the location specified by both the PC and MA.

I.O. RESET When the switch is raised, the I.O. Reset switch clears the control flip-flops, including Busy, Done and Interrupt Disable, in all devices connected to the I/O Bus.

RESET When the switch is depressed, the Reset switch causes a Mains Return condition, i.e. PC and MA will be set to 000002, a Mains Return Interrupt will be pending and all peripherals cleared down as in I/O reset.

MEM-STEP Each time the switch is raised, the processor executes instructions one memory cycle at a time in the state indicated by the phase indicator lights, displaying the MA on the bit-indicator lights, and then stops. The phase indicator lights will then indicate the next phase to be executed.

N.B. The use of the Examine A, B, PC, etc. switches between memory steps within an instruction, can display information without altering the conditions necessary for the successful execution of the remainder of the instruction.

INST.STEP When this switch is depressed, the processor will execute one complete instruction from wherever the PC and MA have previously been set. In other words it will operate from the beginning of a FETCH, completing the current instruction. The address displayed on the bit indicator lights after each Instruction Step is the address of the next consecutive instruction word.

Now follows a description of the 4 toggle switches in the bottom row, right hand side. These are kept in the 'up' position for the normal running of the processor and are only depressed when in use.

AUTO-STEP This switch provides slow speed operation of the Instruction Step (an average of 25 instructions per second).

INT IF MA=SW Having first set an address on the Data switches, this switch may then be depressed; the program is then set to Continue until the MA equals this address, when an internal interrupt is called.

N.B. This equalisation could happen during any machine phase, but the interrupt would not occur until the instruction had been completed.

CONT.INT. When this switch is depressed, an internal interrupt is called after every step, assuming Interrupt is on.

I.O. INT.OFF When this switch is depressed, all Input/Output external interrupts are disabled, (but internal processor interrupts are still enabled).