SOFTWARE SPECIFICATION FOR THE

UNIVERSAL COMMUNICATIONS CONTROLLER

I N T R O D U C T I O N

The **Universal Communications Controller (UCC)** is a microprocessor based system comprising four RS232C compatible serial data ports, which can operate in a variety of data transfer rates and formats while handling line protocols automatically and transparently to the Distributor processor.

Each input/output port has a unique system address defined by a D.I.L. switch setting and six 17 bit data registers for each of the DATO/DATI I/O instructions. A set of BUSY, DONE and INT REQ flags are provided for each of the ports but as each set is active for both input and output data transfers, additional features have been incorporated to enable the Distributor software to identify channel interrupts. These are explained in detail in later sections.

Data transfers may be single or double bytes and in character by character or data channel mode. Output data transfers have a 2 byte buffer whereas input data has a 512 byte holding buffer that can be filled before being serviced by the Distributor.

SOFTWARE OUTLINE

Data transfers and UCC control are accomplished via the 6 DATI/DATO registers, each of which has a specific function as shown below:-

DATO 1	Write data (output)
DATO 2	Initiate data channel mode
DATO 3	Set mode and special commands
DATI 1	Read data (input)
DATI 2	Read data channel address
DATI 3	Read status

Each of the aforementioned modes will effect a data transfer between Distributor and UCC but to make the UCC processor aware of the occurrence of any of them they must be accompanied by a **START** command. This will enable the setting of the BUSY flag which also causes an interrupt condition to the UCC processor.

If the I/O operation can be completed then BUSY will be reset and DONE/INT REQ set to signal this event. If however the operation cannot complete e.g. a DATI 1 command and no data has been input to the UCC, then BUSY will reset and the condition transferred to a status bit in the DATI 3 reg. The channel is thus released for output operations in the normal way.

An ACK INT in response to INT REQ will provide the interrupting channel address on the data highway with bit 7 set to indicate that the input side of the channel is interrupting. The interrupt structure allows channel 1 the highest priority and channel 4 the lowest. Priority between input and output of any channel is first come first served.

INT REQ and DONE flags can be reset by issuing another command in the data transfer mode or with a special DATO 3 mode as detailed later. Use of the CLEAR command should be avoided as this will reset the flags without informing the UCC processor that this has occurred. IOPLS has no function whatsoever on the UCC.

DATA TRANSFERS

DATO 1 - OUTPUT DATA

To output data to a peripheral device the DATO 1 START instruction is used and can transfer one or 2 bytes. If bit 17 of the DATO 1 register is a zero then just the lower byte (bits 1 to 8) will be sent. If bit 17 is a one then 2 bytes will be sent; lower first then upper (bits 9 to 16). If conditions allow, the byte or word will be presented to the serial channel for transmission and then BUSY will reset and DONE and INT REQ will set. ACK INT will cause the channel address to appear on the data highway. This condition can be followed by a further DATO 1 START instruction up to the end of the data transfer. The final operation to clear the interrupt must be a DATO 3 START instruction with bits 17 and 1 set. This will allow the processor to reset the channel. DONE/INT REQ will not occur as a result of the DATO 3 START instruction.

If the data transfer cannot complete because of a line control condition or by reception of a line protocol then BUSY will reset and transfer to bit 10 of the DATI 3 register. When the condition is removed the transfer will complete as normal. A status interrogation during the BUSY state will show both BUSY and TX Disabled bits as detailed later. A reset command using DATO 3 can be used to clear the BUSY state.

A status condition (COMMAND ERROR) will result if further DATO 1 START instuctions are issued whilst the channel is busy.

DATI 1 - INPUT DATA

The instruction DATI 1 START will cause the DATI 1 register contents to be transferred to the Distributor processor and the START will initiate an input cycle on the UCC board. The first data word of a transfer must be discarded and the DONE interrogated for the DATI 1 register to be filled with data proper. If data is available for the Distributor then the normal BUSY reset DONE/INT REQ set routine will follow. However, the response to ACK INT will be bit 7 appended to the channel address to indicate an input channel interrupt.

If no data is available then the BUSY flag will reset and appear as a status bit in the DATI 3 register. As previously described DONE/INT REQ can be reset by successive input instructions but the final operation should be a DATO 3 START instruction using bits 17 and 2.

Data transfers are in single byte mode only with the upper unused bits set to zero.

DATA CHANNEL MODE

DATO 2 START instruction will load the DATO 2 register with an address and set the channel into the data channel mode: bit 17 reset for a data transfer from Distributor to peripheral and bit 17 set for the reverse.

When outputting data, bit 17 of the data will define single or double byte transfers as described for DATO 1 operations whilst on inputs, data will be packed 2 bytes to a word and bit 17 set. The DATI 2 register reflects to current data channel address during the transfer whereas the DATO 2 register remains unchanged and so must be set up for each data channel transfer.

The BUSY flag will reset when the instruction has been initiated and DONE/INT REQ set on completion, which is on receipt of a carriage return (15_8) or after 4096 bytes transferred.

Any data transfer instructions attempted during the data channel mode will be disregarded and cause the COMMAND ERROR status bit.

I/O MODE

The operating mode of each channel is defined by the DATO 3 START instruction. Both bytes of the 17 bit word are used either singly or combined as illustrated below. Bit 8 is used as an enable for the lower byte and bit 16 as an enable for the upper byte. Bit 17 is used to indicate a special command group.

BAUD RATE

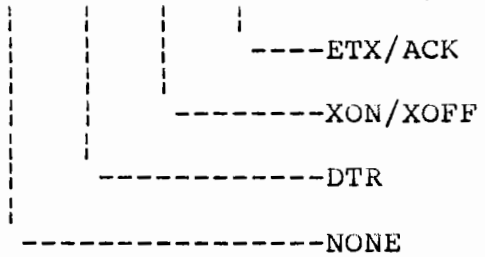
Bit 17 = 0
Bit 16 Upper Byte Enable

Bit 15	0 0 0 0 0 0 0 0	1 1 1 1 1 1 1 1)	
Bit 14	0 0 0 0 1 1 1 1	0 0 0 0 1 1 1 1)	BAUD RATE
Bit 13	0 0 1 1 0 0 1 1	0 0 1 1 0 0 1 1)	
Bit 12	0 1 0 1 0 1 0 1	0 1 0 1 0 1 0 1)	
	A B C D E F G H	**I J K L M N O P**	

A	50	**I**	1800
B	75	**J**	2000
C	110	**K**	2400
D	134.5	**L**	3600
E	150	**M**	4800
F	300	**N**	7500
G	600	**O**	9600
H	1200	**P**	19200

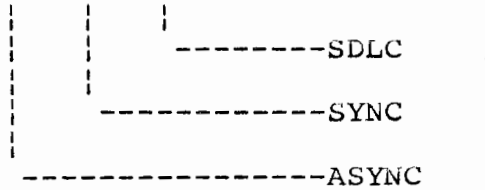
Bit 11 Not Used

Bit 10 0 0 1 1) Line Protocols
Bit 9 0 1 0 1)



Bit 8 Lower Byte Enable

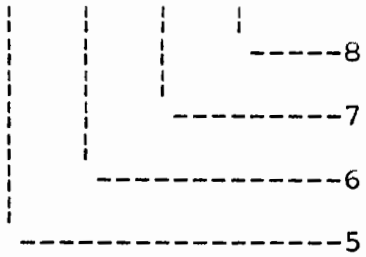
Bit 7 0 1 1
Bit 6 0 0 1



) Future Enhancements

Bit 5	0	=	1 Stop Bit		1	=	2 Stop Bits
Bit 4	0	=	Odd Parity		1	=	Even Parity
Bit 3	0	=	Parity Disabled		1	=	Parity Enabled

Bit 2	0	0	1	1	) Data Bits
Bit 1	0	1	0	1	)



All channels revert to 9600 Baud, Even Parity, 2 stop bits and 7 data bits with XON/XOFF line protocol after IORST or Power on. Each IORST also causes an XON to be transmitted to each device.

At least 5 ms should be allowed after an IORST for the UCC to complete its initialisation before any commands are issued.

SPECIAL COMMAND MODE

DATO 3 START and bit 17 set causes this mode. BUSY will set on receipt of START and will reset without the occurrence of DONE/INT REQ on completion. Bit significance for this mode is as shown below and any bit combination may be used.

Bit 17 On

Bit 4 Reset Tx Channel
Bit 3 Reset RX Channel - clear data buffer and status
Bit 2 Reset Tx DONE/INT REQ condition
Bit 1 Reset Rx DONE/INT REQ condition

STATUS WORD

A DATI 3 instruction will result in the current channel status being transferred. START need not accompany this instruction, in which case BUSY/DONE flags will not be disturbed. The status word is as defined below.

Bit 1	- Rx Disabled	This could be as a result of line protocols (XOFF) or absence of the DCD line on the interface. It will reset when either condition allows.
Bit 2	- Tx Disabled	This could be as a result of line protocols (ETX) or absence of the CTS line on the interface. It will reset when ACK is received or CTS goes active.
Bit 3	- I/P Buffer Overflow	This bit shows data lost as a result of incompatible line protocols being used between UCC and device.
Bit 4	- Data Channel Mode	
Bit 5	- Rx Parity)	All these conditions result in a "?" being passed to the Distributor in place of the received characters. They are reset by the clear Rx special command.
Bit 6	- Rx Overrun)	
Bit 7	- Rx Frame Error)	
Bit 8	- Rx Buffer not Empty - or Data available in the I/P Buffer	
Bit 9	- Rx BUSY)	Indicates the channel has been started and waiting for completion
Bit 10	- Tx BUSY)	
Bit 16	- Command Error -	I/O instructions issued to busy channel

Bits 11 through 15 are unused and set to zero.